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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,841	09/25/2003	Maximino Aguilar JR.	AUS920030699US1	8312
40412 7590 04/09/2008 IBM CORPORATION- AUSTIN (JVL) C/O VAN LEEUWEN & VAN LEEUWEN PO BOX 90609 AUSTIN, TX 78709-0609				
EXAMINER				
WALERIC CHARLES				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/670,841

**Applicant(s)**

AGUILAR ET AL.

**Examiner**

ERIC C. WAI

**Art Unit**

2195

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 January 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3-11, 13-21 and 23-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-11, 13-21 and 23-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SF/08)  
Paper No(s)/Mail Date 12/27/2007.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. Claims 1, 3-11, 13-21, and 23-30 are presented for examination.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 11, and 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.
4. Claims 1, 11, and 21 recite in lines 14-15, "wherein the second scheduler schedules the second tasks concurrently with when the first scheduler schedules the first tasks", and in lines 19-20, "wherein the first scheduler and the second scheduler are both located on a first processor that is the first type of processor". Since schedulers are also threads, it is unclear how both schedulers can be concurrently executing on the same processor. Furthermore, Applicant's remarks dated 01/18/2008 assert support in the specification in Figures 43, 46, and corresponding text. However, an examination of the specification provides no support that the scheduling is performed concurrently, only that scheduling does indeed occur.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 11, and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- a. The following terms are not clearly understood in the claims:

- i. Claims 1, 11, and 21 recite in lines 14-15, "wherein the second scheduler schedules the second tasks concurrently with when the first scheduler schedules the first tasks", and in lines 19-20, "wherein the first scheduler and the second scheduler are both located on a first processor that is the first type of processor". Since schedulers are also threads, it is unclear how both schedulers can be concurrently executing on the same processor.

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1, 3-11, 13-21, and 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCrory (US Pat No. 6,513,057) in view of Correnti et al. (US Pat No. 5,394,547).

9. McCrory was disclosed on IDS dated 10/02/2007.

10. Regarding claim 1, McCrory teaches a method for multithreading tasks in a computer environment that includes a plurality of dissimilar processors (col 2 lines 27-30), said method comprising:

scheduling operation of a plurality of first tasks adapted to be executed by a first type of processor (col 2 lines 48-52), the scheduling performed by a first scheduler that maintains a first run queue that includes data corresponding to the first tasks (col 2 lines 48-52);

in response to the scheduling operation of the plurality of first tasks by the first scheduler, inserting the plurality of first tasks in the first run queue (col 7 lines 44-47);

scheduling operation of a plurality of second tasks adapted to be executed by a second type of processor (col 2 lines 48-52), the scheduling performed by a scheduler that maintains a second run queue that includes data corresponding to the second tasks (col 2 lines 48-52), wherein the second scheduler schedules the second tasks concurrently with when the first scheduler schedules the first tasks (col 4 lines 24-26, wherein the OS provides scheduling);

in response to the scheduling operation of the plurality of second tasks by the second scheduler, inserting the plurality of second tasks in the second run queue (col 7 lines 44-47); and

wherein the first scheduler and the second scheduler are both located on a first processor that is the first type of processor (col 3 lines 1-4, wherein the OS scheduler is

a single mode binary code file which can only be executed on one of the processor families).

11. McCrory differs from the claimed invention by teaching symmetrically multi threading as opposed to asymmetrically multithreading. However, McCrory's method will asymmetrically multithread when single mode binary code for two different family of processors needs to be scheduled. McCrory's symmetrically multithreading refers to the scheduling of mixed mode binary code on two families of processors.

12. McCrory also differs from the claimed invention by not explicitly teaching that the second scheduler is different from the first scheduler.

13. Correnti teaches a method of utilizing different schedulers in an operating system kernel (abstract, col 2 lines 30-33). Correnti teaches that such a method is useful to optimize system resource allocation (col 1 lines 60-64). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify McCrory to utilize different schedulers for each of the first and second tasks. One would be motivated by the desire to increase the efficiency of system resource allocation as taught by Correnti.

14. Regarding claim 3, McCrory and Correnti do not explicitly teach that the scheduling operation of the plurality of first tasks is asymmetric to the scheduling operation of the plurality of second tasks.

15. It would have been obvious to one of ordinary skill in art at the time of the invention that the scheduling operation is asymmetric since the processor families operate independently of each other.

16. Regarding claim 4, McCrory teaches that a first identifier space corresponds to the first type of processor and wherein a second identifier space corresponds to the second type of processor; and wherein a first task list corresponds to the first type of processor and wherein a second task list corresponds to the second type of processor (col 2 lines 64-67, wherein the OS determines the processor family based on the binary code stream).

17. Regarding claim 5, McCrory teaches that the scheduling operation of the plurality second tasks further comprises:

receiving a new task from the plurality of second tasks (col 7 lines 26-29);

identifying new task attributes corresponding to the new task (col 7 lines 41-43, wherein the priority of a thread is determined);

comparing the new task attributes with one or more scheduled task attributes (col 7 lines 41-43, wherein priority of threads are compared), the

scheduled task attributes corresponding to one or more scheduled tasks that are included in the second run queue (col 7 lines 41-43, wherein threads are scheduled by priority); and

performing the scheduling of the new task based upon the comparing (col 7 lines 41-43, wherein threads are scheduled by priority).

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18. Regarding claim 6, McCrory teaches that at least one of the new task attributes are selected from the group consisting of a policy and a priority (col 7 lines 41-43).

19. Regarding claim 7, McCrory teaches informing the second type of processor to load one of the second tasks in response to the scheduling (col 3 lines 10-12, wherein notifications are sent).

20. Regarding claim 8, McCrory teaches that the computer environment includes a plurality of second type of processors (col 2 line 50, family of processors).

21. However, McCrory does not teach wherein the second scheduler maintains a plurality of second run queues, each of the plurality of second run queues corresponding to each of the plurality of second type of processors.

22. It would have been obvious to one of ordinary skill in the art at the time of the invention, to modify McCrory to include a queue for each of the processors. One would be motivated by the desire to schedule each processor individually instead of the scheduling the group as a whole.

23. Regarding claim 9, McCrory and Correnti do not teach that the scheduling operation of the plurality of second tasks further comprises: receiving a new task from the plurality of second tasks analyzing a plurality of workloads that correspond to the plurality of second type of processors; identifying an available second type of processor from the plurality of second type of processors in response to the analyzing; and



including the new task in the second run queue from the plurality of second run queues that corresponds to the available second type of processor.

24. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to analyze the load at each processor. One would be motivated by the desire to perform load balancing among all the processors to increase the efficiency of McCrory and Correnti.

25. Regarding claim 10, McCrory and Correnti do not teach that the first type of processor is a processing unit and wherein the second type of processor is a synergistic processing unit.

26. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a synergistic processing unit. One would be motivated by the desire to extend the breath of McCrory.

27. Regarding claims 11, and 13-20, they are the system claims of claims 1, and 3-10 above. Therefore, they are rejected for the same reasons as claims 1, and 3-10 above.

28. Regarding claims 21, and 23-30, they are the computer program product claims of claims 1, and 3-10 above. Therefore, they are rejected for the same reasons as claims 1, and 3-10 above.

***Response to Arguments***

29. Applicant's arguments with respect to claims 1, 3-11, 13-21, and 23-30 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric C. Wai whose telephone number is 571-270-1012. The examiner can normally be reached on Mon-Thurs, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng - Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eric C Wai/  
Examiner, Art Unit 2195

/Lewis A. Bullock, Jr./  
Supervisory Patent Examiner, Art Unit 2193